

Model Name: GA-B85M-DS3H

Revision 3.0

SHEET

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12	PCH GPIO,CTRL,AUDIO
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SHEET

TITLE

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Gigabyte Technology

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Revision 3.0

Component value change history

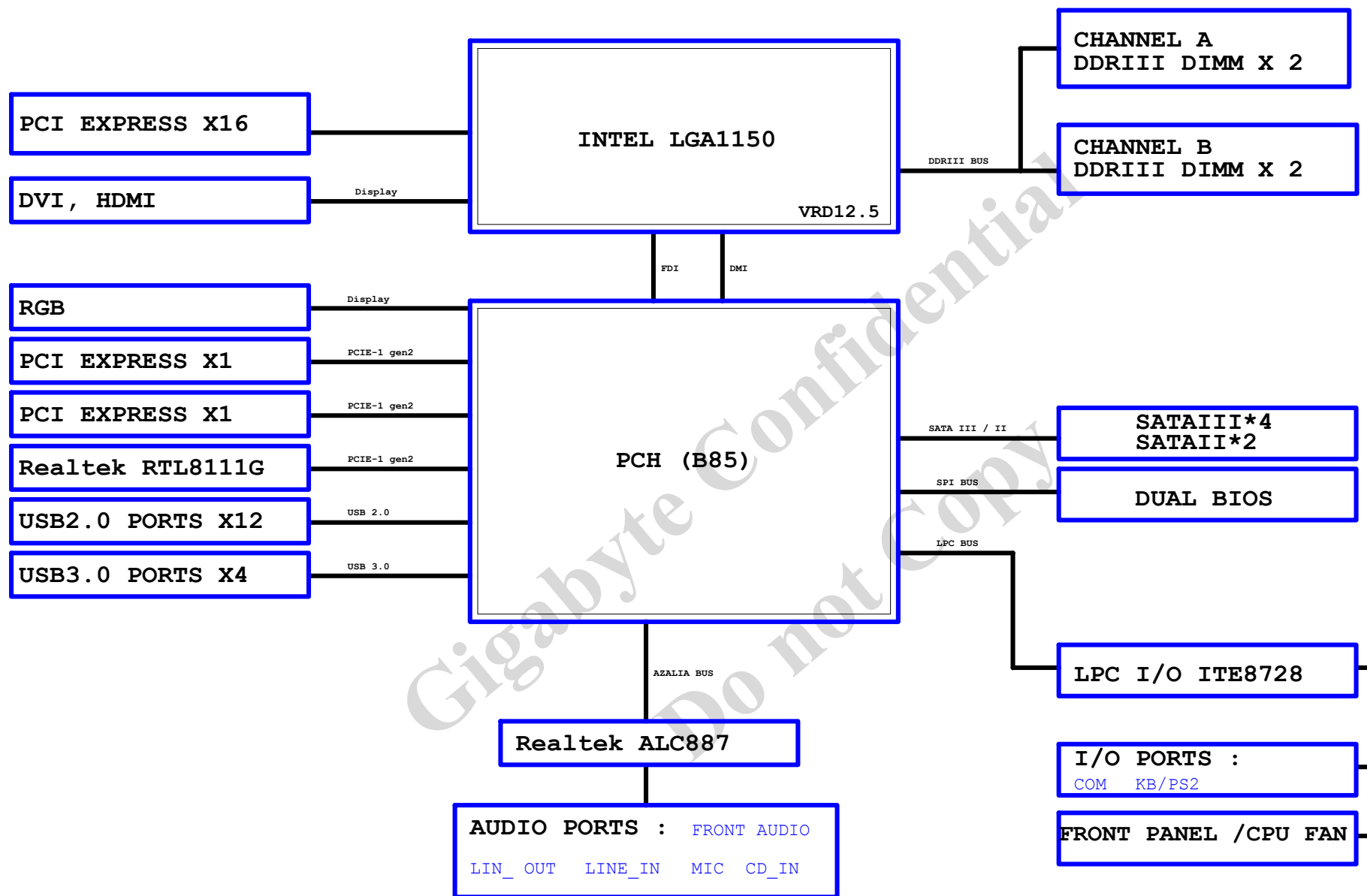
2014/07/31

Data	Change Item	Reason
2013/06/28	ADD RSMRST DELAY	
2013/08/13	Update Rev to 1.1	
	PCIE X16 New Footprint "PCIESLOT-164DN-Q-1"	
2013/08/23		EBOM: 9M85MDS3H-00-11A
2013/09/13	Update to R1.11	
	Follow Crystal Trace Rule	
	SYS_FAN, DDR 0ohm 0402 -> 0603	
	Update Fuse 1206 Footprint "POLYSWITCH-1206-1"	
	Update PPAK Footprint "Q_TDS0N8-GDS-T"	
2013/10/22	NX1: 25M/20p -> 12p	PBOM: 9M85MDS3H-00-11B
	NC7, NX8: 27p -> 10p	
2013/11/04	NC7, NX8: 10p -> 15p	PBOM: 9M85MDS3H-00-11C
2013/11/05	Update to R1.12	PBOM: 9M85MDS3H-00-11D
	Modify NX1 Trace	
2013/11/27	MR17 0ohm -> 0603 FUSE(10FP5-06100B-00R)	PBOM: 9M85MDS3H-00-11E
	ALC887 強壯版 (10HP5-368870-32R)	
2014/02/17	Sales Costdown Rev2.0	
	CPU Power ISL95820 1U2D -> ISL95812 1U1D	
	DVI Non-Level Shift	
	BIOS Size 64M -> 32M	
2014/02/20	SBA線路OPTION,整合電阻成排阻,精簡線路	
2014/02/24	整合電阻成排阻	
2014/02/27	MASK/DEL CAP	
2014/03/07	ADD ESD : NC3,NC4 (22P)	
2014/03/11	NR6改SHT PAD	
2014/03/12	WBC28,30,25,27,31解開MASK	
	COM:BLACK,F_AUDIO:GRAY	
	DEL後窗AUDIO 180P	

Circuit or PCB layout change

[illegible]

BLOCK DIAGRAM



(E)



FDI_TXP[0..1] >> FDI_TXP[0..1] [9]
FDI_TXN[0..1] >> FDI_TXN[0..1] [9]

(C)

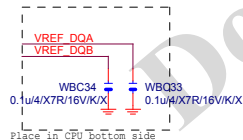
-CPURST

Title				CPU LGA1150-A			
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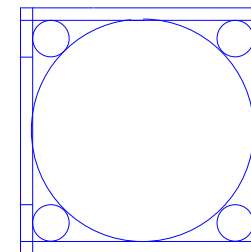
LGA1150A	
MAAA0 AU13	DDR0_MA0
MAAA1 AV16	DDR0_MA1
MAAA2 AU16	DDR0_MA2
MAAA3 AW17	DDR0_MA3
MAAA4 AU17	DDR0_MA4
MAAA5 AW18	DDR0_MA5
MAAA6 AW17	DDR0_MA6
MAAA7 AT18	DDR0_MA7
MAAA8 AU18	DDR0_MA8
MAAA9 AT19	DDR0_MA9
MAAA10 AW11	DDR0_MA10
MAAA11 AV19	DDR0_MA11
MAAA12 AU19	DDR0_MA12
MAAA13 AY10	DDR0_MA13
MAAA14 AT20	DDR0_MA14
MAAA15 AU21	DDR0_MA15
MODT_A0 AW10	DDR0_ODT0
MODT_A1 AY3	DDR0_ODT1
MODT_A2 AW9	DDR0_ODT2
MODT_A3 AU8	DDR0_ODT3
AW33	DDR0_ECC0
AW33	DDR0_ECC1
AU31	DDR0_ECC2
AU31	DDR0_ECC3
AT33	DDR0_ECC4
AU33	DDR0_ECC5
AT31	DDR0_ECC6
AW31	DDR0_ECC7
SBA00 <- SBAA0 AV12	DDR0_BA0
SBA01 <- SBAA1 AT11	DDR0_BA1
SBA02 <- SBAA2 AT21	DDR0_BA2
CKEA0 <- CKEA0 AV22	DDR0_CKE0
CKEA1 <- CKEA1 AT23	DDR0_CKE1
CKEA2 <- CKEA2 AU22	DDR0_CKE2
CKEA3 <- CKEA3 AU23	DDR0_CKE3
CSA0 <- CSA0 AU14	DDR0_CS_N0
CSA1 <- CSA1 AV9	DDR0_CS_N1
CSA2 <- CSA2 AU10	DDR0_CS_N2
CSA3 <- CSA3 AW8	DDR0_CS_N3
DCLKA0 <- DCLKA0 AY15	DDR0_CLK_P0
DCLKA0 <- DCLKA0 AY16	DDR0_CLK_N0
DCLKA1 <- DCLKA1 AW15	DDR0_CLK_P1
DCLKA1 <- DCLKA1 AV15	DDR0_CLK_N1
DCLKA2 <- DCLKA2 AW14	DDR0_CLK_P2
DCLKA2 <- DCLKA2 AW14	DDR0_CLK_N2
DCLKA3 <- DCLKA3 AW13	DDR0_CLK_P3
DCLKA3 <- DCLKA3 AY13	DDR0_CLK_N3
AW12	RSVD
RSVD	
SRASA <- SRASA AU12C	DDR0_RAS*
SWEA <- SWEA AU11C	DDR0_WE*
AV20C	RSVD
AW27C	RSVD
SCASA <- SCASA AU9C	DDR0_CAS*
WR61 <- W4/SH1/TMX AK22C	DDR_RESET*
W4	0.1u4/X7R/16V/K/X

HASWELL[10SC1-F01150-11R_10SC1-F01150-12R]

LGA1150B	
MAAB0 AL19	DDR1_MA0
MAAB1 AK23	DDR1_MA1
MAAB2 AM22	DDR1_MA2
MAAB3 AM23	DDR1_MA3
MAAB4 AP23	DDR1_MA4
MAAB5 AL23	DDR1_MA5
MAAB6 AY24	DDR1_MA6
MAAB7 AV25	DDR1_MA7
MAAB8 AU26	DDR1_MA8
MAAB9 AW25	DDR1_MA9
MAAB10 AP18	DDR1_MA10
MAAB11 AY25	DDR1_MA11
MAAB12 AV26	DDR1_MA12
MAAB13 AR15	DDR1_MA13
MAAB14 AV27	DDR1_MA14
MAAB15 AY28	DDR1_MA15
MODT_B0 AM17	DDR1_ODT0
MODT_B1 AL18	DDR1_ODT1
MODT_B2 AM16	DDR1_ODT2
MODT_B3 AK15	DDR1_ODT3
AM26	DDR1_ECC0
AM25	DDR1_ECC1
AP25	DDR1_ECC2
AP26	DDR1_ECC3
AL26	DDR1_ECC4
AL25	DDR1_ECC5
AR26	DDR1_ECC6
AR25	DDR1_ECC7
SBA00 <- SBAB0 AK17	DDR1_BA0
SBA01 <- SBAB1 AL18	DDR1_BA1
SBA02 <- SBAB2 AW28	DDR1_BA2
CKEB0 <- CKEB0 AW29	DDR1_CKE0
CKEB1 <- CKEB1 AY29	DDR1_CKE1
CKEB2 <- CKEB2 AU28	DDR1_CKE2
CKEB3 <- CKEB3 AU29	DDR1_CKE3
CSB0 <- CSB0 AP17	DDR1_CS_N0
CSB1 <- CSB1 AN15	DDR1_CS_N1
CSB2 <- CSB2 AM17	DDR1_CS_N2
CSB3 <- CSB3 AL15	DDR1_CS_N3
DCLKB0 <- DCLKB0 AM20	DDR1_CLK_P0
DCLKB0 <- DCLKB0 AM21	DDR1_CLK_N0
DCLKB1 <- DCLKB1 AP22	DDR1_CLK_P1
DCLKB1 <- DCLKB1 AP21	DDR1_CLK_N1
DCLKB2 <- DCLKB2 AN20	DDR1_CLK_P2
DCLKB2 <- DCLKB2 AN21	DDR1_CLK_N2
DCLKB3 <- DCLKB3 AP19	DDR1_CLK_P3
DCLKB3 <- DCLKB3 AP20	DDR1_CLK_N3
SCASB <- SCASB AP18C	DDR1_CAS*
SRASB <- SRASB AL20	RSVD
SWEB <- SWEB AK18C	DDR1_RAS*
VREF_DOA <- VREF DOA AB39	DDR_VREF_DO0
VREF_DOB <- VREF DOB AB40	DDR_VREF_DO1
AE34	MDB0
AE35	MDB1
AG35	MDB2
AH35	MDB3
AD34	MDB4
AG35	MDB5
AH34	MDB7
AL34	MDB8
AL35	MDB9
AK31	MDB10
AL31	MDB11
AK34	MDB12
AK35	MDB13
AK32	MDB14
AL32	MDB15
AN34	MDB17
AP34	MDB21
AN31	MDB19
AP31	MDB23
AN35	MDB20
AP35	MDB16
AN32	MDB18
AP32	MDB22
AM29	MDB25
AM28	MDB28
AR29	MDB27
AR28	MDB30
AL28	MDB24
AL28	MDB29
AP29	MDB26
AP28	MDB31
AR12	MDB32
AL13	MDB33
AL12	MDB35
AR13	MDB36
AP13	MDB37
AM13	MDB38
AM12	MDB39
AR9	MDB45
AP9	MDB41
AR6	MDB47
AP6	MDB43
AR10	MDB44
AP10	MDB40
AR7	MDB46
AP7	MDB42
AM9	MDB52
AL9	MDB53
AL6	MDB50
AL7	MDB55
AM10	MDB48
AL10	MDB49
AM6	MDB54
AM7	MDB51
AH6	MDB61
AH7	MDB60
AE6	MDB59
AE7	MDB63
AJ6	MDB56
AJ7	MDB57
AF6	MDB58
AF7	MDB62
AF36	DQS80
AL33	DQS81
AP33	DQS82
AN28	DQS83
AN12	DQS84
AP8	DQS85
AL8	DQS86
AG7	DQS87
AN25	DQS80
AK33	DQS81
AN33	DQS82
AN29	DQS83
AN13	DQS84
AR8	DQS85
AM8	DQS86
AG6	DQS87
AN26	DQS80



HASWELL[10SC1-F01150-11R_10SC1-F01150-12R]

CR
CPU RETENTION/X

LGA1150_P



ILM_BP/1156/CSP/LM_BP/1156/CSP[12KRC-0F0001-52R_12KRC-0F0001-51R]

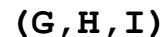
DDR BUS

[7] MODT_A[0..3]	<-	MODT_A[0..3]
[8] MODT_B[0..3]	<-	MODT_B[0..3]
[7] MDA[0..63]	<-	MDA[0..63]
[8] MDB[0..63]	<-	MDB[0..63]
[7] DQSA[0..7]	<-	DQSA[0..7]
[7] -DQSA[0..7]	<-	-DQSA[0..7]
[7] MAA[A0..15]	<-	MAA[A0..15]
[8] MAAB[0..15]	<-	MAAB[0..15]
[8] DQSB[0..7]	<-	DQSB[0..7]
[8] -DQSB[0..7]	<-	-DQSB[0..7]

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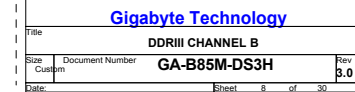
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CPU LGA1150-B			
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(F, J)



Title			
CPU LGA1150-C			
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(B)



DMI:12/4/4/4/12 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

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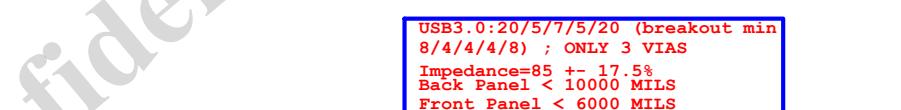
-----PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)-----

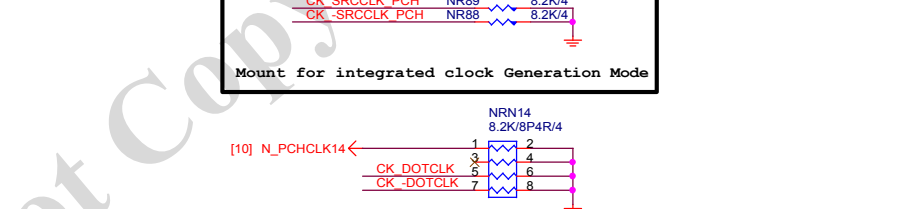
```

PCHJ

PCHB

B85: Port 6/7 N/A
H81: Port 6/7/12/13 N/A





11

CD, HEATCIN



OC[7:4]# for Device 26 (ports 8-13)

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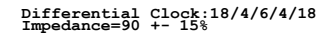
PCH FDI DMI USB PCIE NVRAM

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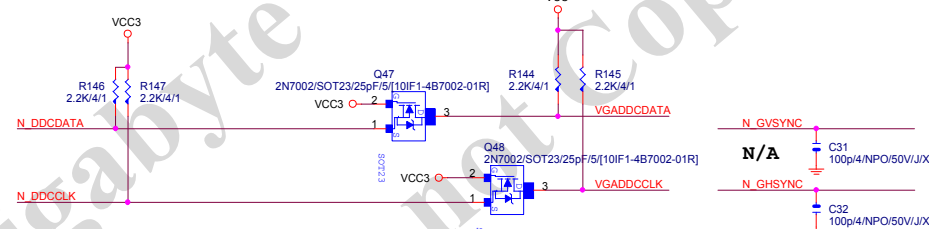
(E)



(G)



N -CLK GND NR42 8.2K/4
 N CLK GND NR41 8.2K/4



BLACK CONNECTOR

N R
N G
N B

R152 75/4/1
R150 75/4/1
R151 75/4/1
C34 10pF/4/NPO/50V/J/X
C36 10pF/4/NPO/50V/J/X
C35 10pF/4/NPO/50V/J/X

Close to Filter

FB1 60/4/3A/S
FB2 60/4/3A/S
FB3 60/4/3A/S

N/A

C37 22pF/4/NPO/50V/J/X
C38 22pF/4/NPO/50V/J/X
C39 22pF/4/NPO/50V/J/X

VGA R
VGA G
VGA B

SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

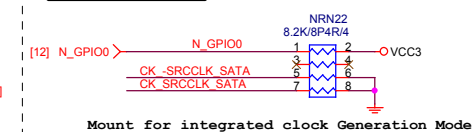
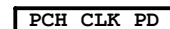


Diagram illustrating the N-SATA0 pinout configuration:

Pin	Signal	Internal Connection
1	GND	
2	N_SATA0TXP	NC44
3	N_SATA0TXN	NC43
4	T+	
5	N_SATA0RXN	NC38
6	N_SATA0RXP	NC37
7	GND	

[illegible]

Diagram illustrating the N-SATA4 controller structure, showing four parallel data paths (TXP, TXN, RXN, RXP) connected to a common output bus (GND, T+, T-, R-).

Input	Output
N SATA4TXP	1
N SATA4TXN	2
N SATA4RXN	3
N SATA4RXP	4

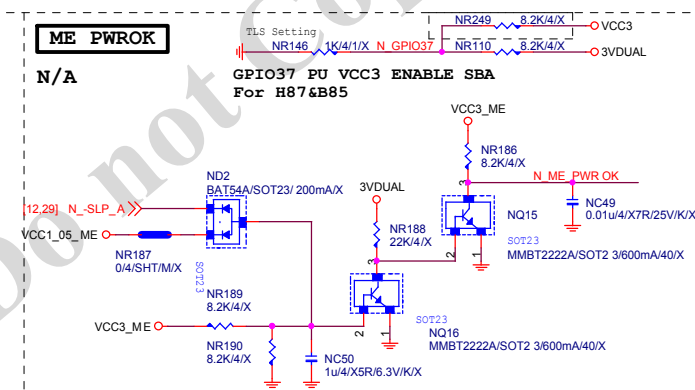
N SATA1TXP	SHORT4- MASK/X	NC42	N SATA1TXPC	1	GND
N SATA1TXN	SHORT4- MASK/X	NC41	N SATA1TXNC	2	T+
				3	T-
				4	GND
N SATA1RXN	SHORT4- MASK/X	NC40	N SATA1RXNC	5	R-
N SATA1RXP	SHORT4- MASK/X	NC39	N SATA1RXP	6	R+
				7	GND

Diagram showing the pin connections for SATA3TXP, SATA3TXN, SATA3RXN, and SATA3RXP signals. The signals are connected to pins 1 through 7, with ground connections at pins 2, 3, 4, 6, and 7.

Signal	Pin	Connection
N SATA3TXP	1	NC34
N SATA3TXN	2	NC33
N SATA3RXN	3	NC32
N SATA3RXP	4	NC31
N SATA3TXP	5	NC34
N SATA3TXN	6	NC33
N SATA3RXN	7	NC32
N SATA3RXP	8	NC31

N SATA5TXP	NC57	SHORT4-MASK/X	N SATA5TXPC	1	
N SATA5TXN	NC56	SHORT4-MASK/X	N SATA5TXNC	2	
				3	
				4	
N SATA5RXN	NC55	SHORT4-MASK/X	N SATA5RXNC	5	
N SATA5RXP	NC54	SHORT4-MASK/X	N SATA5RXP	6	

ME PWROK



N/A

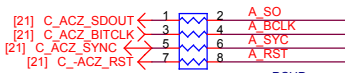
The diagram shows a circuit for the N/A pin. A resistor labeled **MASK** NR184 2K4/X is connected between pin [12] N_GPIO60 and the gate of an NQ13 MOSFET. The MOSFET is a NQ13 MASK/MMBT2222A/SO T23/600mA/40/X SOT23. Its gate is connected to N_GPIO38, its source is connected to ground, and its drain is connected to N_GPIO60.

Gigabyte Technology

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PCH HOST , SATA, PCI			
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PCH

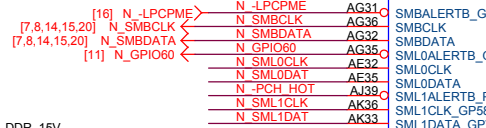
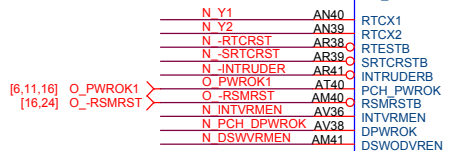
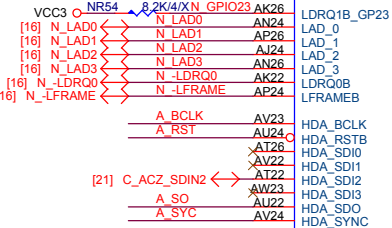
(D)



NRN15 33/8P4R/4

PCHD

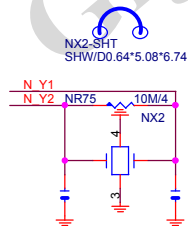
[16] N_LAD[0..3] << N_LAD[0..3]



HSW STRAP13

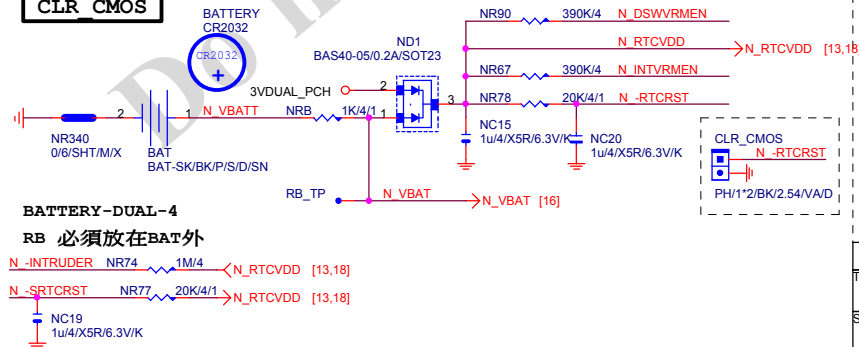
N/A

32.768KHZ



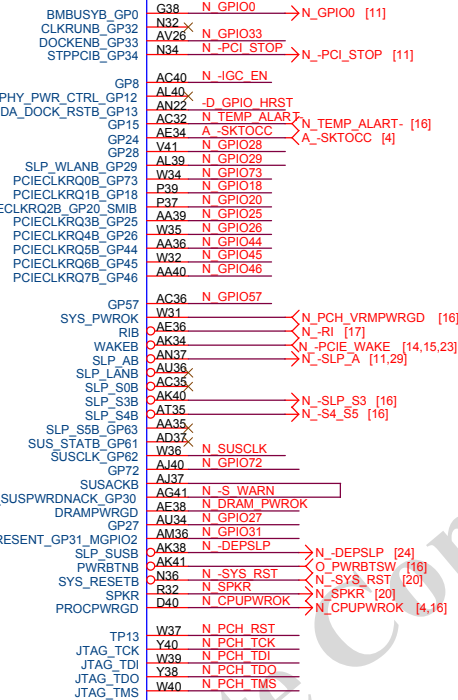
XTALS-RH-N

CLR CMOS

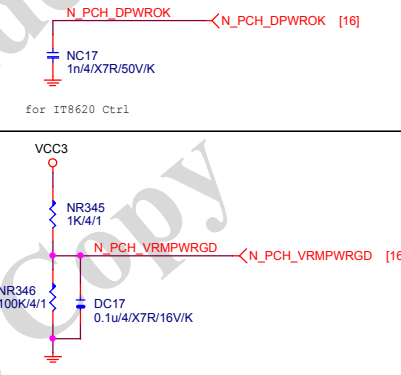


ACZ SDOUT

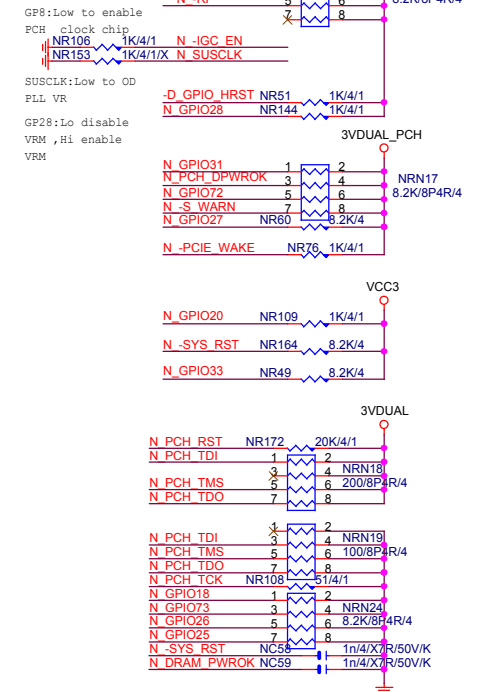
N/A



PCH DPWROK



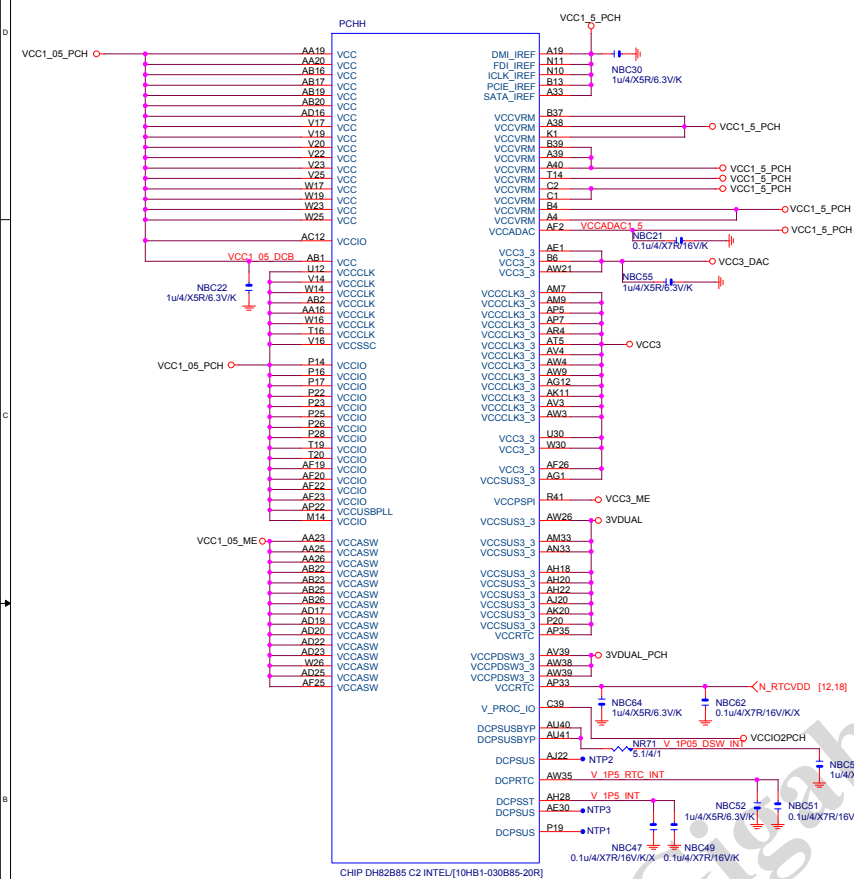
PCH PU/PD



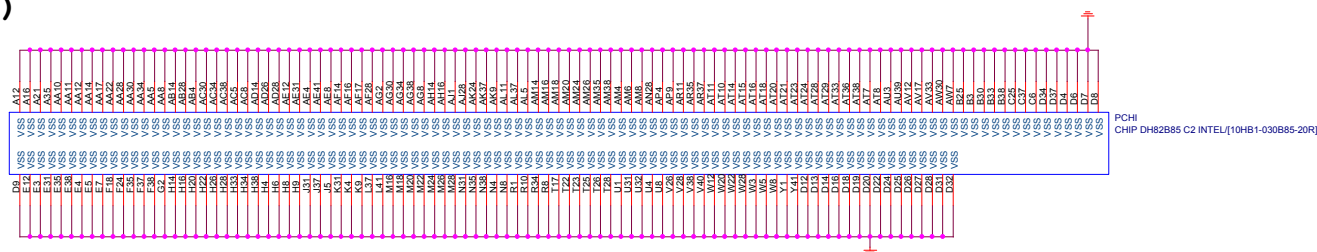
Gigabyte Technology

Title				PCH GPIO , CTRL , AUDIO	
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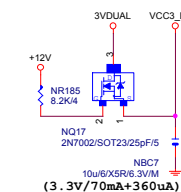
PCH (H)



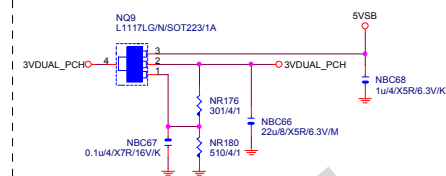
PCH (I)



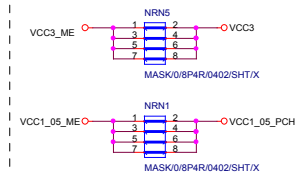
VCC3 DAC



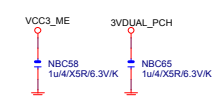
3VDUAL PCH



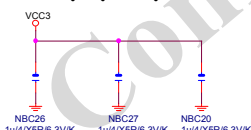
SHT PWR



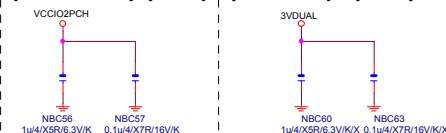
CAP



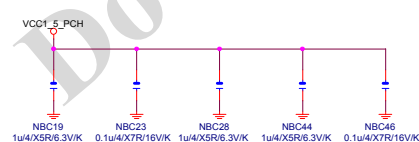
(3.3V) (X3)



► (1.05V)(x2) (3.3V) (x2)

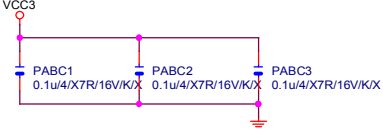


(1.5V) (x5)

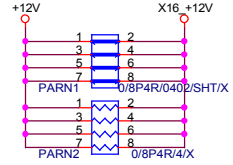


PCIEX16 CAP

N/A



PCIEX16 PROTECT SHT



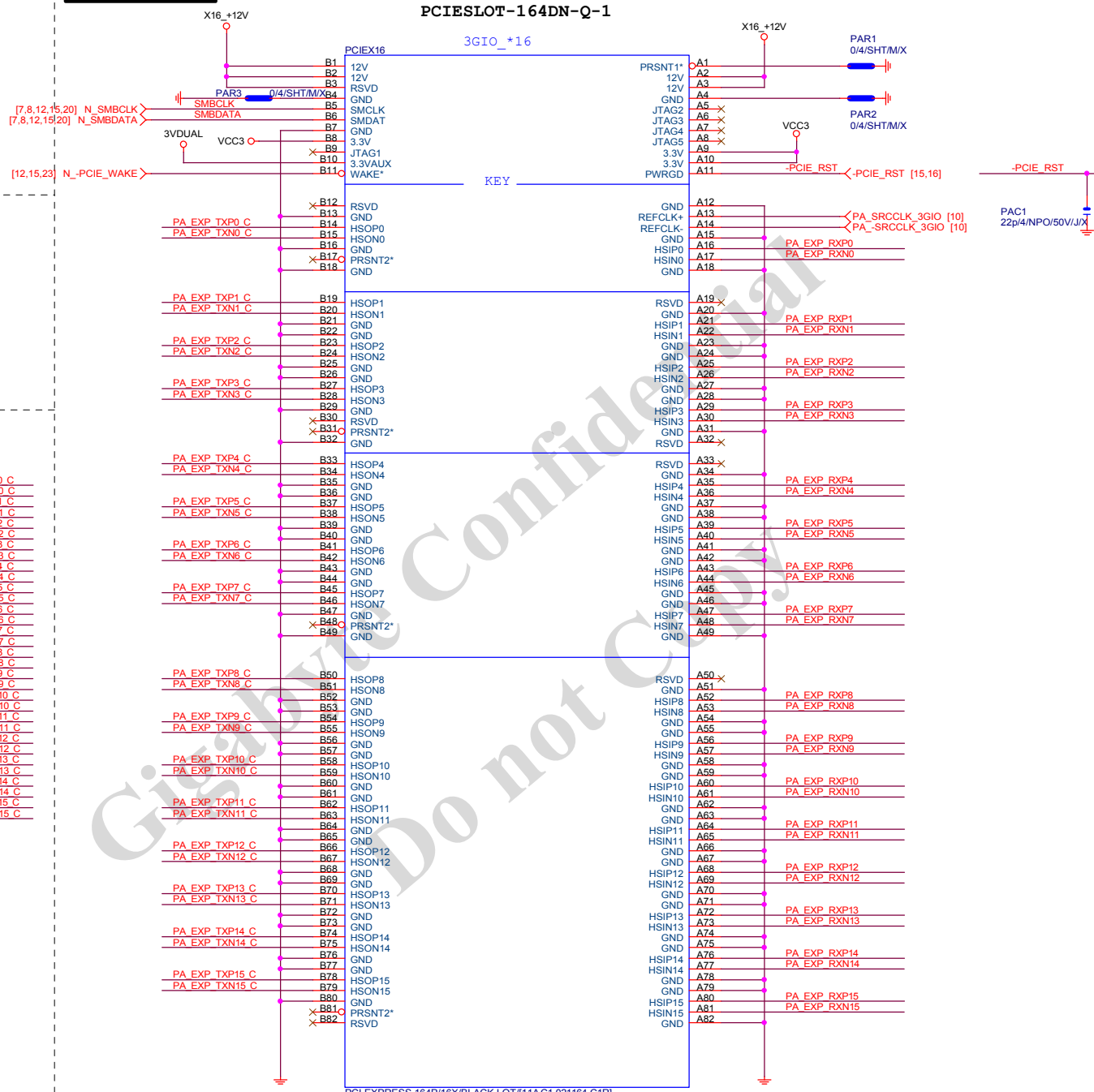
PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PA EXP RXP0_15] >>>PA_EXP_RXP[0..15] [4]
PA EXP RXN0_15] >>>PA_EXP_RXN[0..15] [4]
PA EXP TXP0_15] >>>PA_EXP_TXP[0..15] [4]
PA EXP TXN0_15] >>>PA_EXP_TXN[0..15] [4]

PCIEX16 SLOT

PCIESLOT-164DN-Q-1



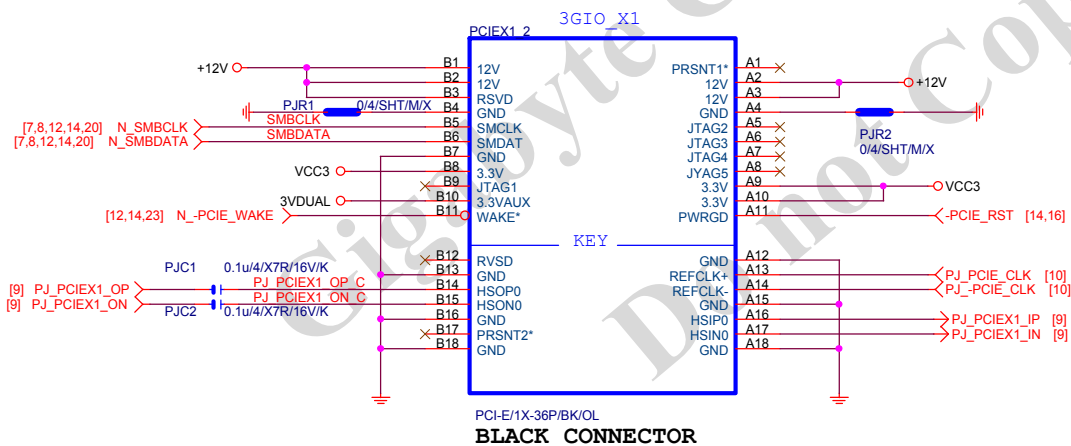
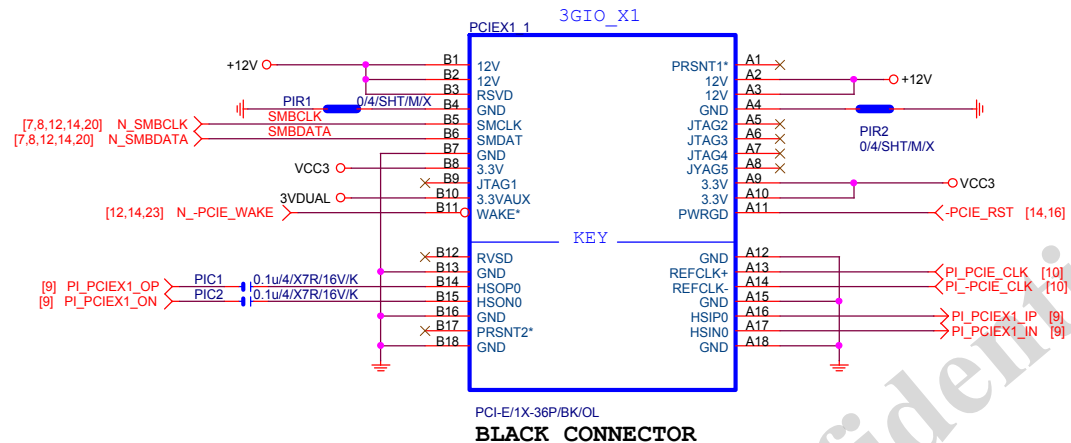
PCI EXPRESS 164P/16X/BLACK LOT/[11AC1-021164-C1R]

BLACK CONNECTOR

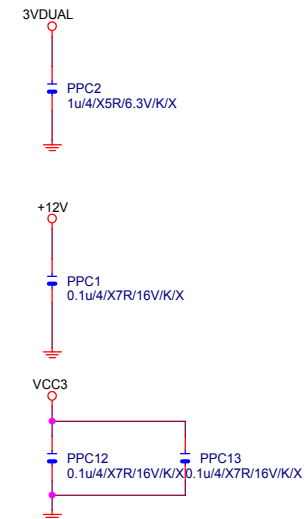
Gigabyte Technology

Title			PCI EXPRESS * 16		
Size	Document Number	GA-B85M-DS3H			Rev 3.0
Custom					
Date:		Thursday, September 11, 2014			
		Sheet 14 of 30			

PCIEX1 SLOT



N/A



Gigabyte Technology

PCI EXPRESS X 1 PORT

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SIO IT8620

-PROCHOT

DUAL BIOS OPT STRAP

SIO CAP

N/A

IT8620E_BX

DUAL BIOS OPT STRAP

SIO 18V

FIX ATX 插拔漏電

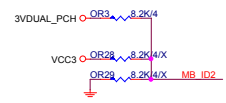
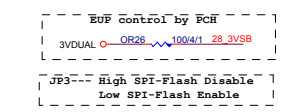
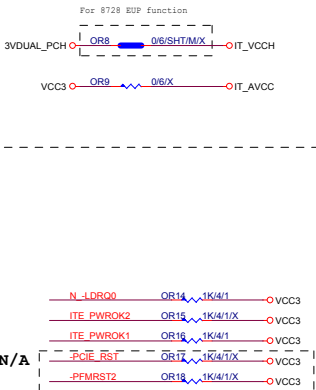
PWR SHT

SIO PU

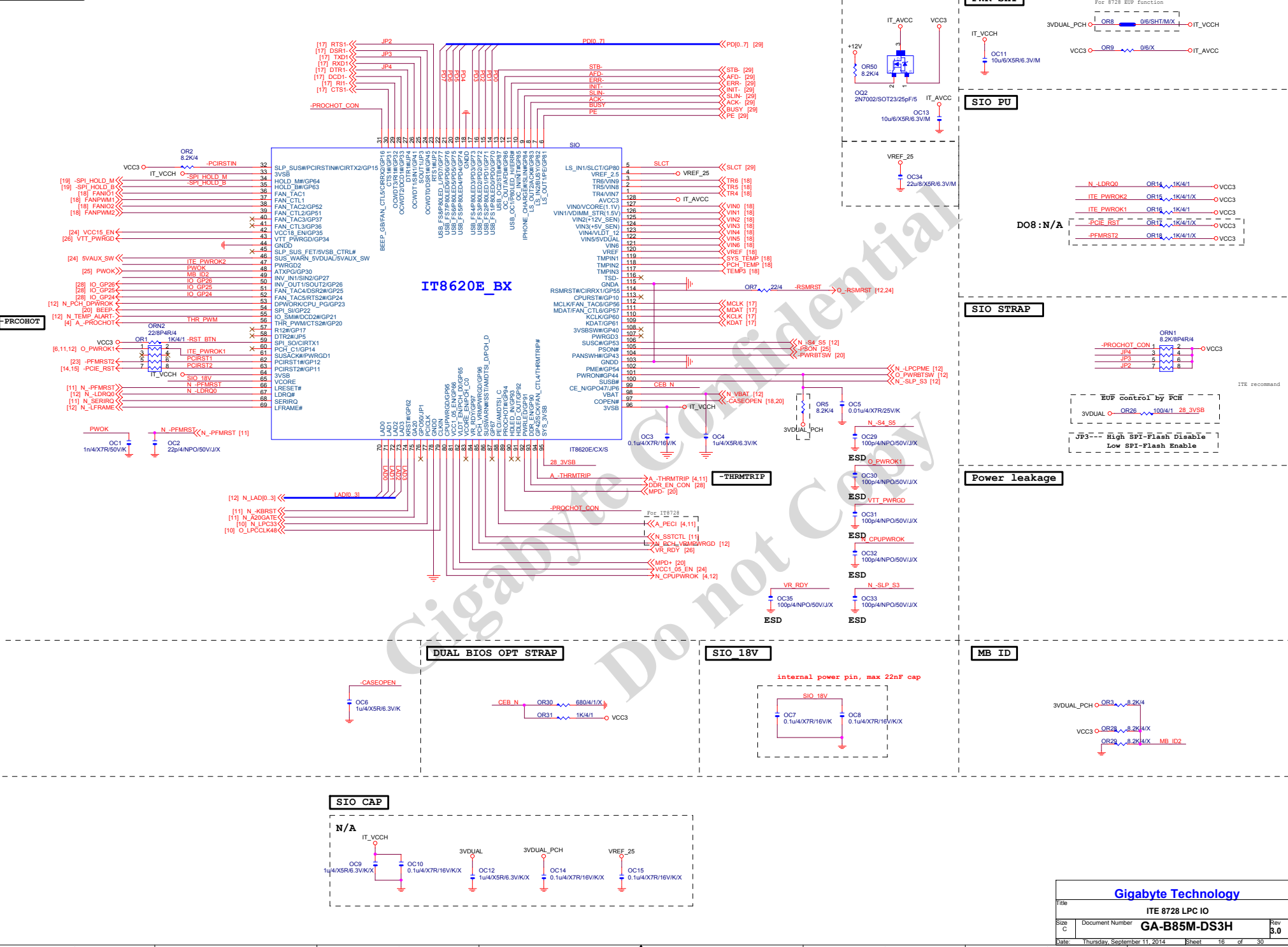
SIO STRAP

Power leakage

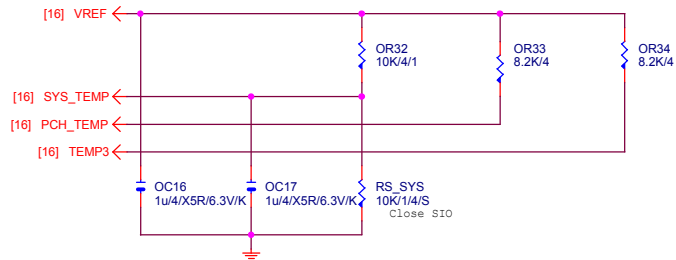
MB ID



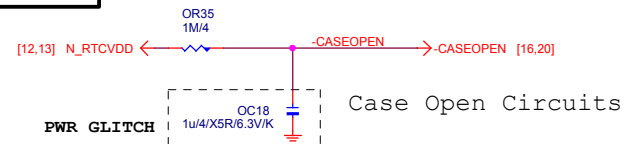
Gigabyte Technology			
Title ITE 8728 LPC IO			
Size C	Document Number	GA-B85M-DS3H	
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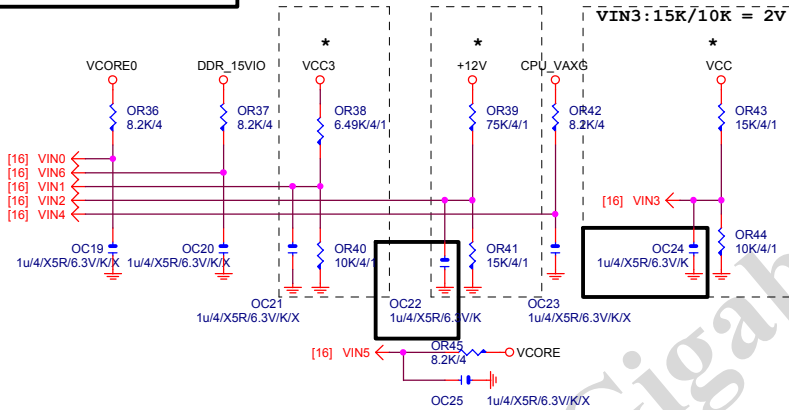
TEMP H/W MONITOR



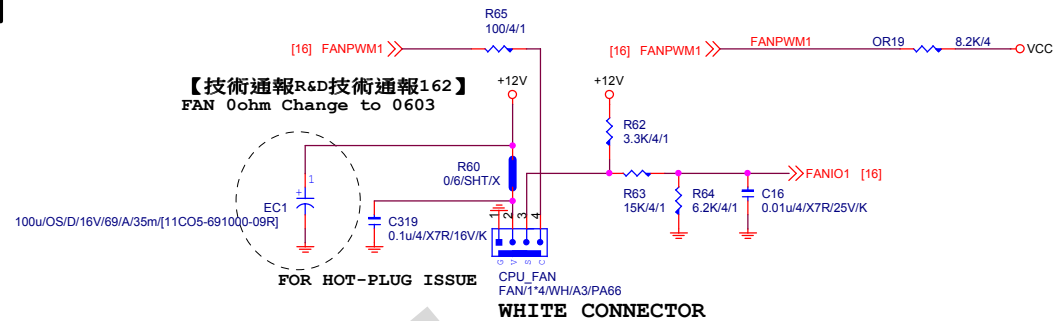
CASE OPEN



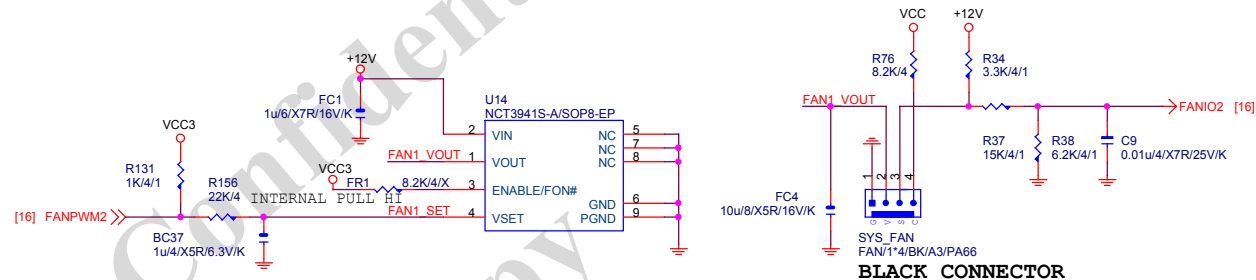
VOLTAGE-- H/W MONITOR



CPU SMART FAN

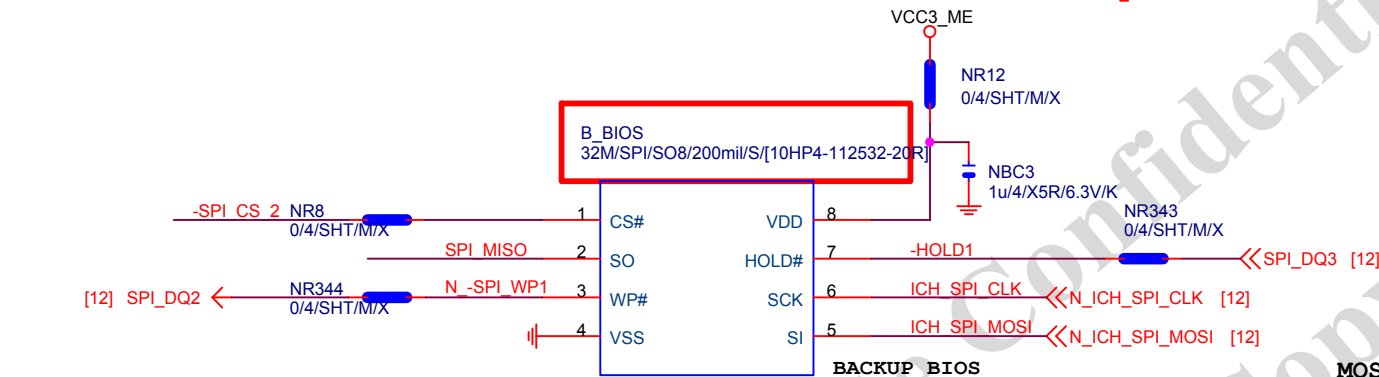
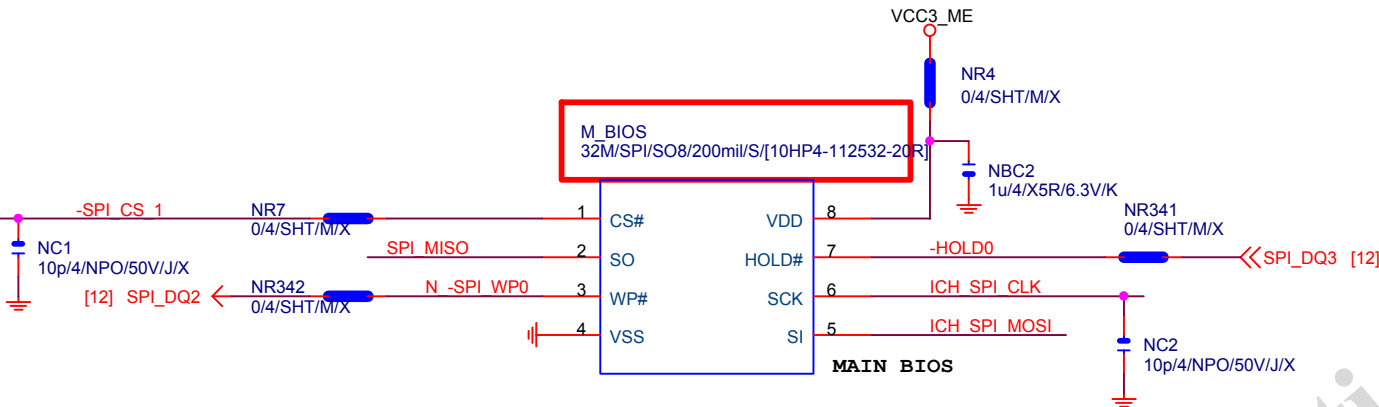


SYS SMART FAN



Gigabyte Technology

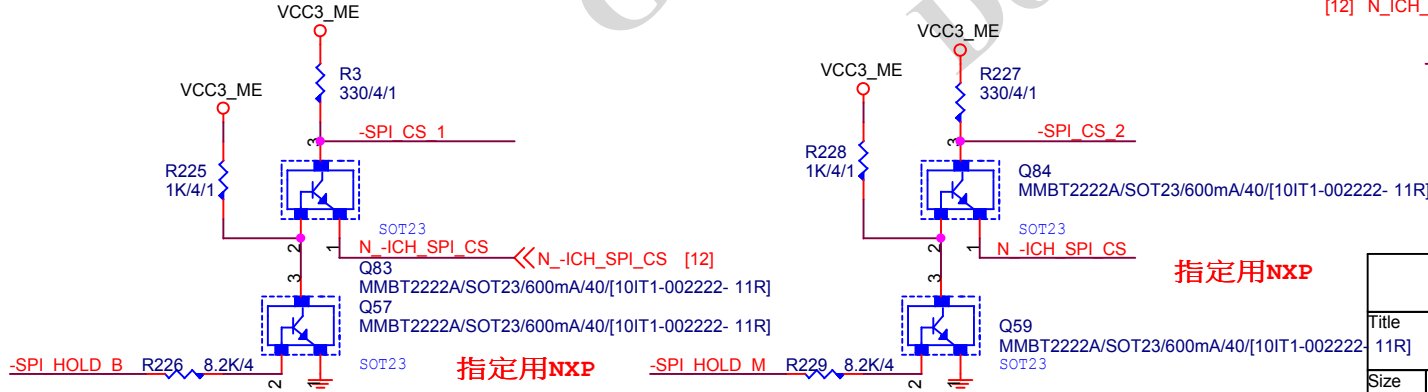
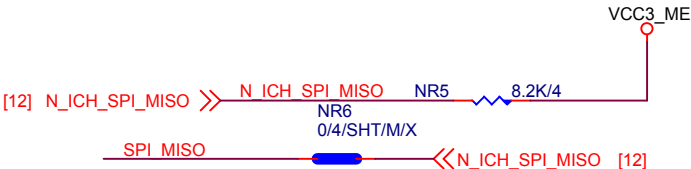
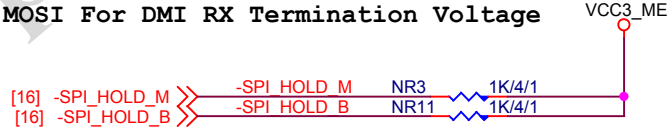
Title			HWM,FAN CTRL,OV
Size	Document Number	GA-B85M-DS3H	
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BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

MOSI For DMI RX Termination Voltage



指定用NXP

Gigabyte Technology

DUAL BIOS

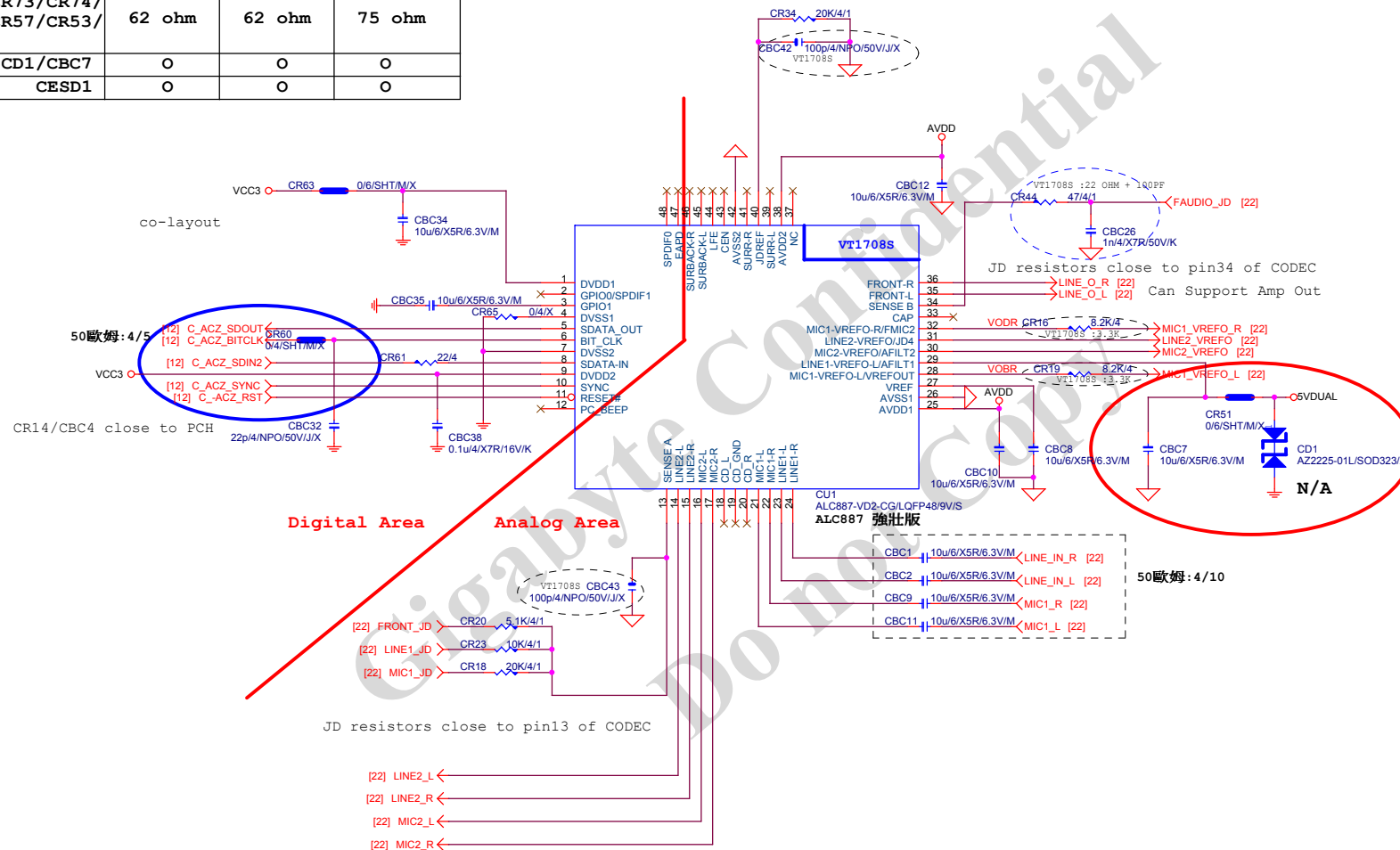
GA-B85M-DS3H

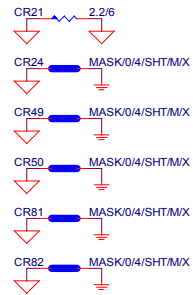
Rev
3.0

Title	11R
Size	Custom
Document Number	GA-B85M-DS3H
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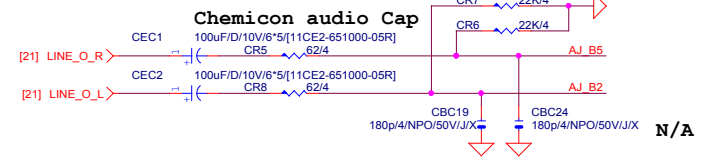
AZALIA CODEC ALC892/ALC887-VD2/VT1708-CE Colay

	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	O	O	O





LINE-OUT



LINE-IN

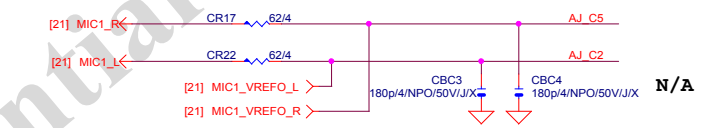
Verify MIC function
in LINE-in

Only reserved for ALC888

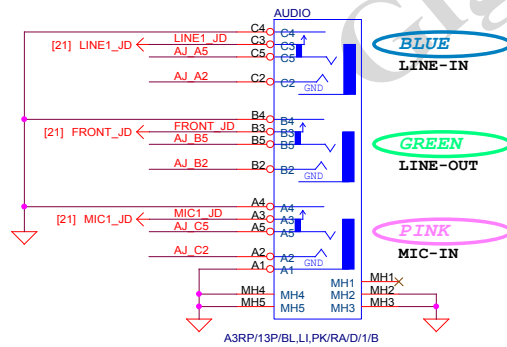


MIC-IN

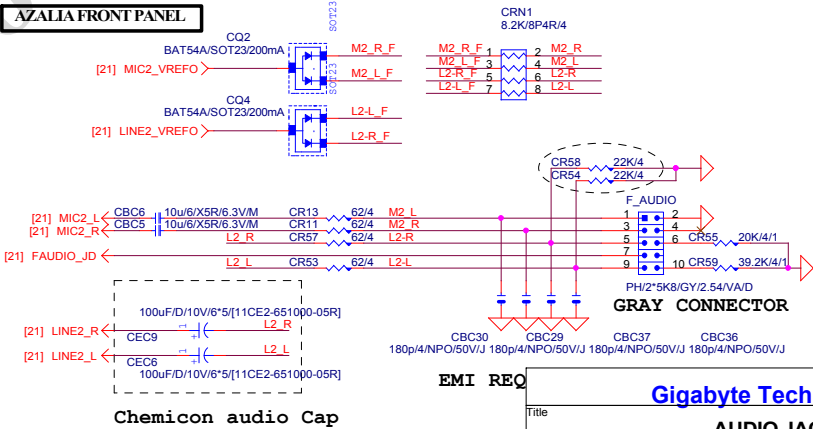
For 889A/888



SPDIF_OUT



AZALIA FRONT PANEL



Gigabyte Technology

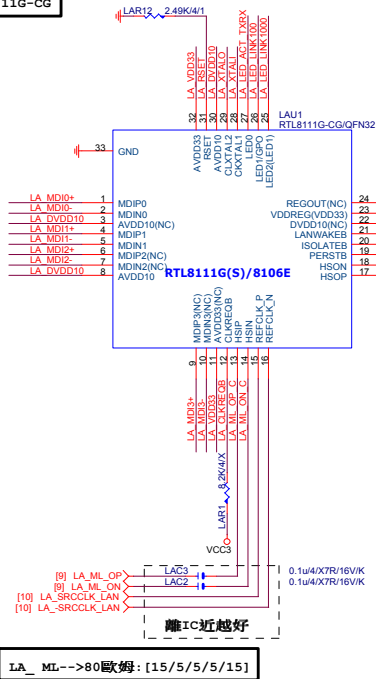
AUDIO JACK

GA-B85M-DS3H

Rev
3.0

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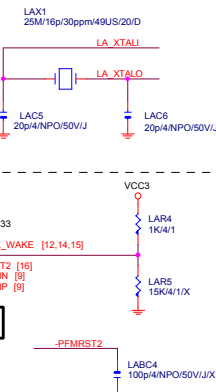
LAN RTL8111G-CG



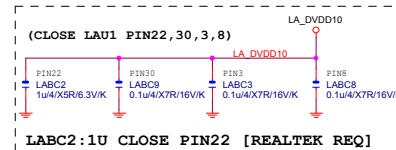
SRCCLK-->50歐姆: [18/4/10/4/18]

離IC近越好

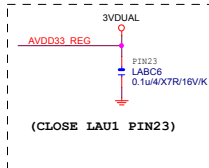
LA_ML-->80歐姆: [15/5/5/5/15]



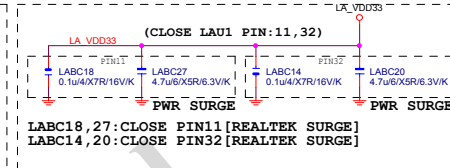
LAN POWER



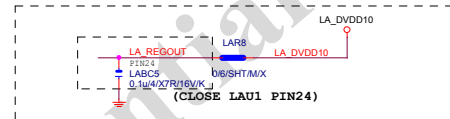
LABC2:1U CLOSE PIN22 [REALTEK REQ]



(CLOSE LAU1 PIN23)



LABC18,27:CLOSE PIN11 [REALTEK SURGE]
LABC14,20:CLOSE PIN32 [REALTEK SURGE]



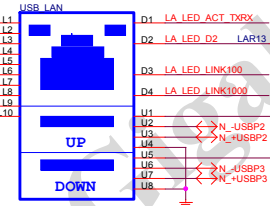
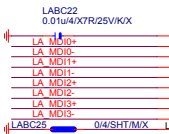
NOTE:
RT8106E: PIN3, 11, 22, 24-->NC
LABC2LABC3, LABC5, LABC18, LABC27-->N/A

BOM NOTICE

料號 規格 廠商
11NR6-702009-96R 1G LAN (12core) UDE (RU9 ESD+)
[LED獨立走線, 可省略外加AZC099料件LAESD1]
1. 9KV ESD BOM:
USB LAN (RU9): 11NR6-702009-96R
2. 28KV ESD BOM:
USB LAN (RU9): 11NR6-702009-96R
LAESD2, LAESD3: 上件AZC398-04S

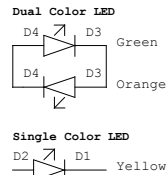
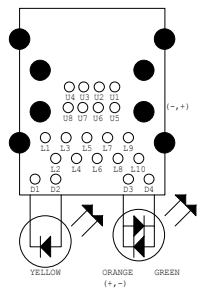
USB LAN CONNECTOR

LA_MDI-->100歐姆: [20/4/8/4/20]



USB+LAN/G/GQ,Y/OB/RA/D1/1/SUR[11NR6-702009-Z1R]
Surge加強RJ45 connector

★
使用RU9 USB_LAN可省略LAESD1保護LED



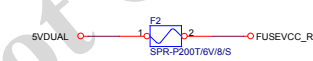
注意: USB PORT (目前: 暫代6,7PORT)
USB-->90歐姆: [15/4.5/7.5/4.5/15]

BOM NOTICE

料號 規格 廠商
11NR6-702009-96R 1G LAN (12core) UDE (RU9 ESD+)
[LED獨立走線, 可省略外加AZC099料件LAESD1]
1. 9KV ESD BOM:
USB LAN (RU9): 11NR6-702009-96R
2. 28KV ESD BOM:
USB LAN (RU9): 11NR6-702009-96R
LAESD2, LAESD3: 上件AZC398-04S

USB X3 POWER

FUSE-0805



EMI SHORT PAD

PS: 視EMI需求



Gigabyte Technology

Realtek RTL8111G

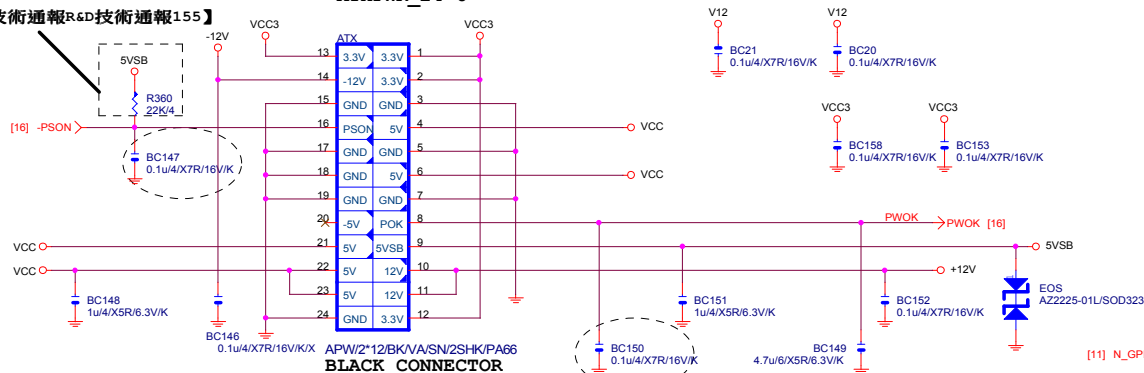
GA-B85M-DS3H

Rev 3.0

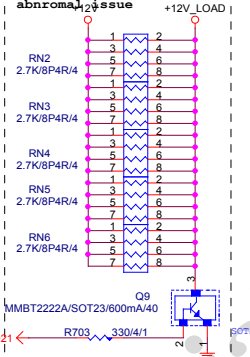
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【技術通報R&D技術通報155】

APW/2*12/BK/VA/12/SH/K/PA66
BLACK CONNECTOR



To fix 12V light load
abnromal issue +12V



The diagram shows a 2x4 pin connector with the following pin configurations:

1	GND	+12V	5
2	GND	+12V	6
3	GND	+12V	7
4	GND	+12V	8

Wires are connected to pins 1, 2, 3, and 4. Pin 1 is connected to a ground symbol. Pin 2 is connected to a common ground line. Pin 3 is connected to a common ground line. Pin 4 is connected to a common ground line. Pins 5, 6, 7, and 8 are connected to a common +12V line.

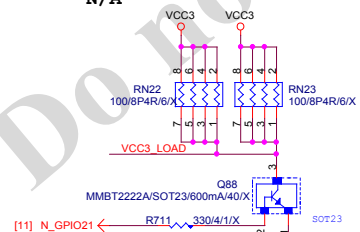
BLACK CONNECTOR

W_X12V_24
W12/4/BK/OC/P14.2/VA/NS/NO/H

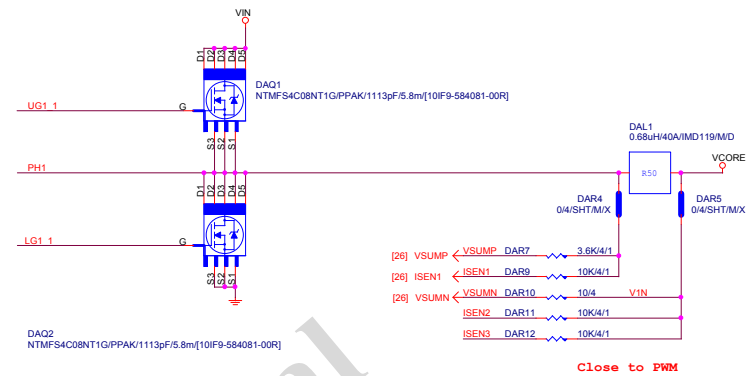
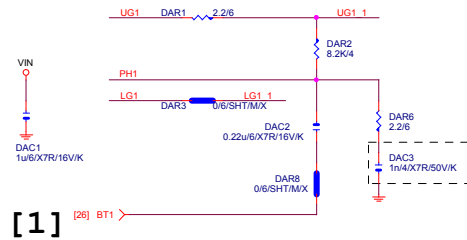
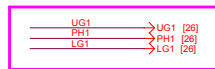
To prevent the 5VSB under loading when boot

【技術通報R&D技術通報154】

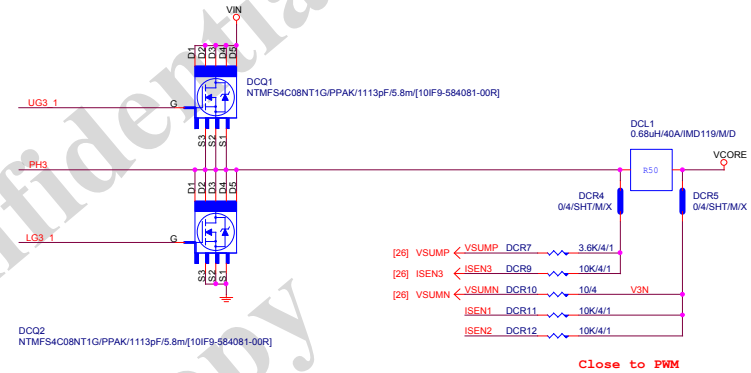
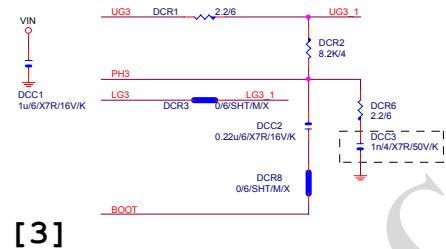
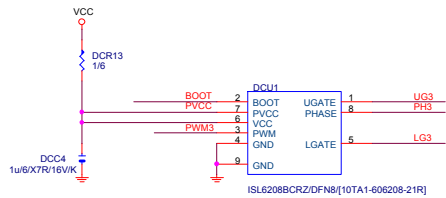
FIX PWR MINMUN LOAD
N/A



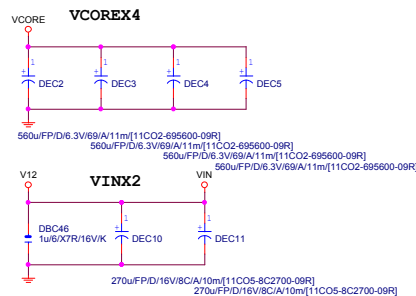
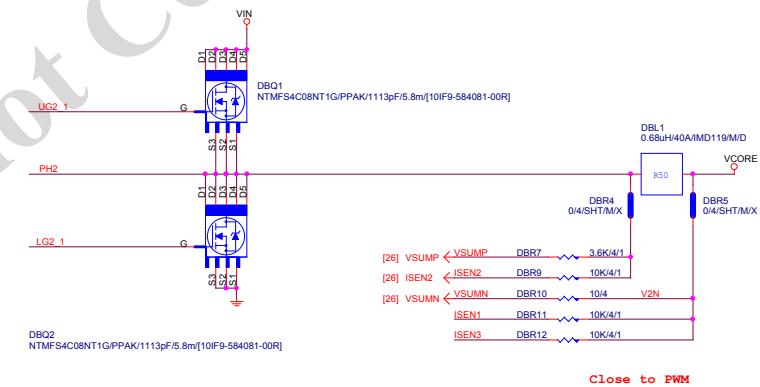
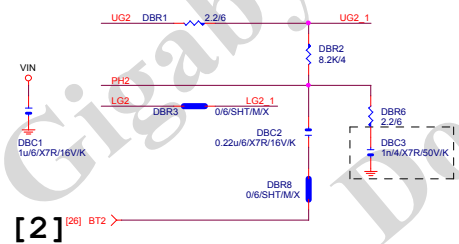
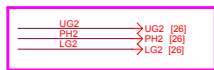
PHASE 1



PHASE 3

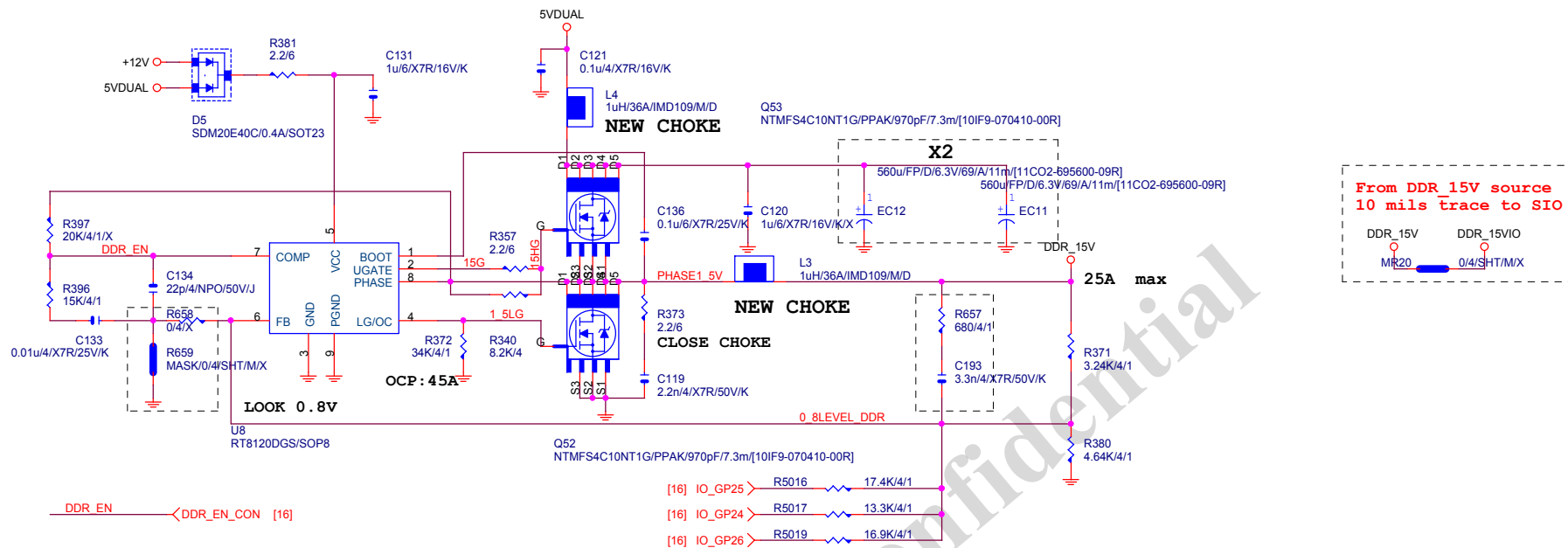


PHASE 2



Gigabyte Technology			
File		CPU CORE VR-2	
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DDR15V



PWR SEQ

GP26	H	L	L	L
GP25	H	H	L	H
GP24	H	H	H	L
	1.35V	1.50V	1.65V	1.70V

VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1

IRMS=11.45A

560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A

Coefficient=1.7 (85°C), 1 (105°C)

VIN Ripple current=4.7X1.7=7.99A (85°C)

-->故固態電容須 $2 \times 7.99 = 15.98 > 11.45A$

$$\text{Rocset} = (\text{Iocp} * \text{Lgate}, \text{rdson}) / \text{Iocset}$$

$$R_{ocset} = (45A * 6.7m\Omega) / 10\mu A = 30K$$

Iocset=10uA

Gigabyte Technology

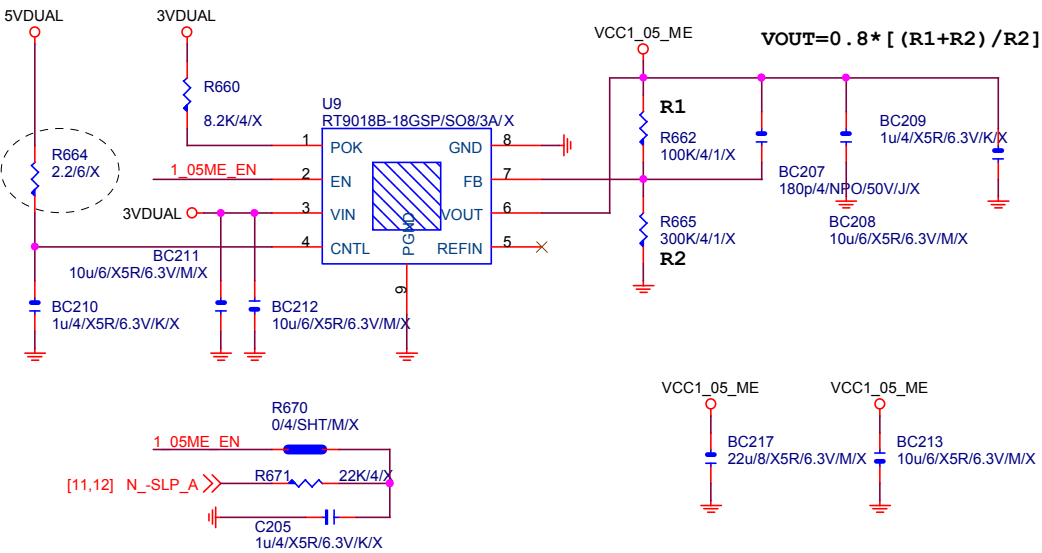
DDR POWER

Size Custom	Document Number GA-B85M-DS3H	Rev 3.0
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VCC1_05_ME

N/A



Second source

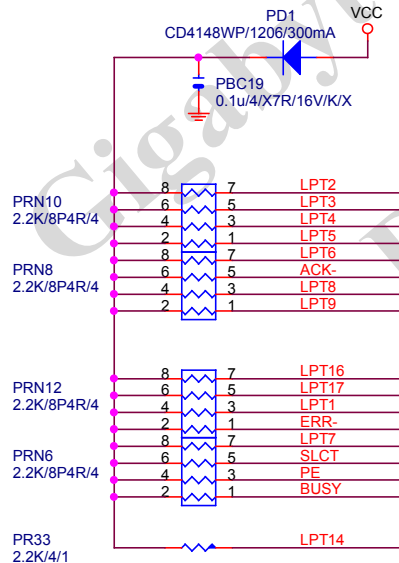
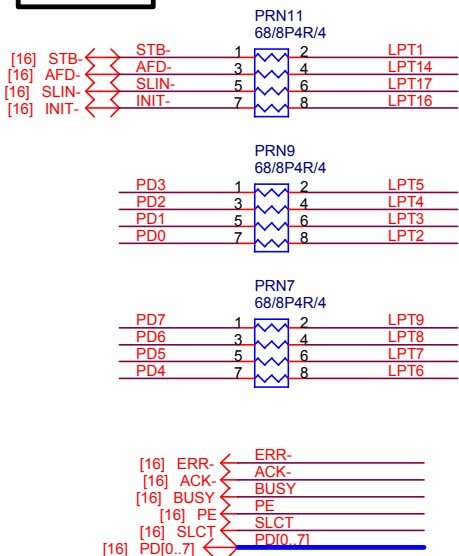
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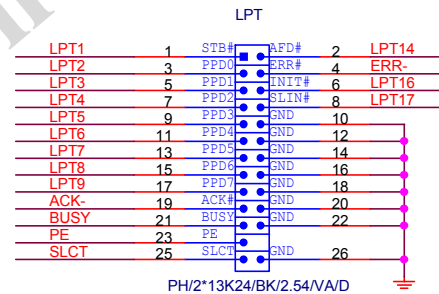
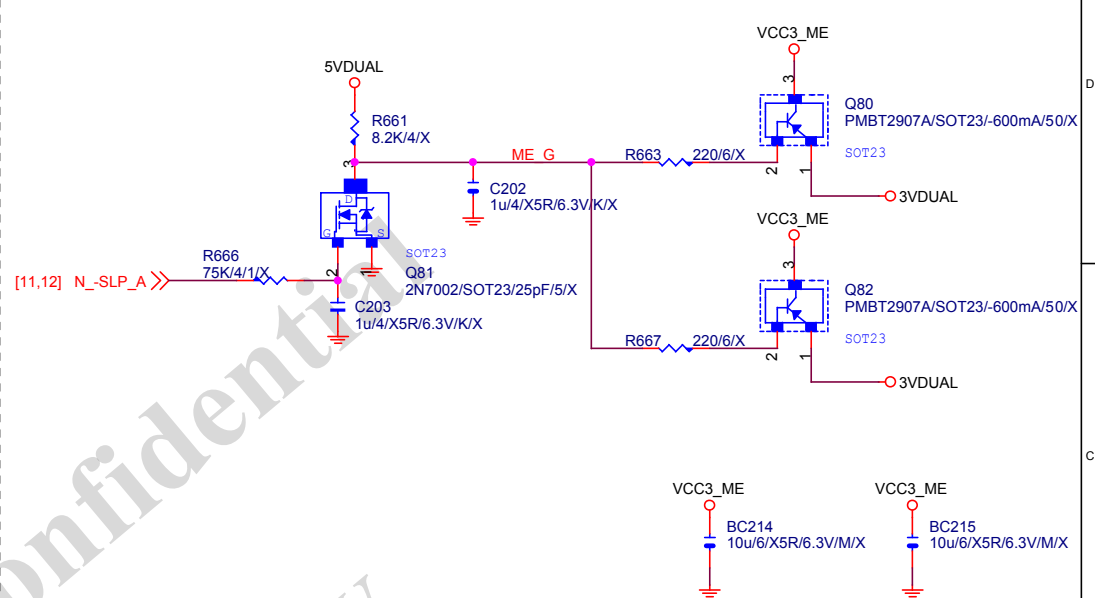
【技術通報R&D技術通報151】
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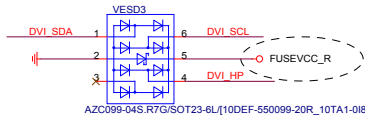
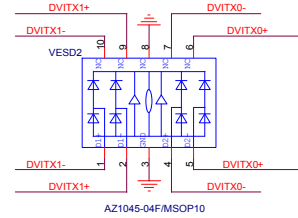
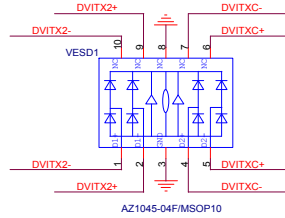
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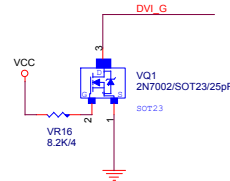
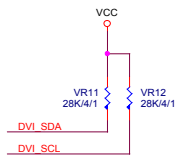
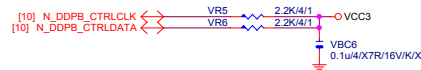
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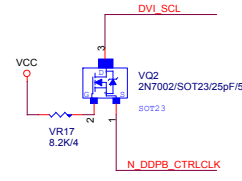
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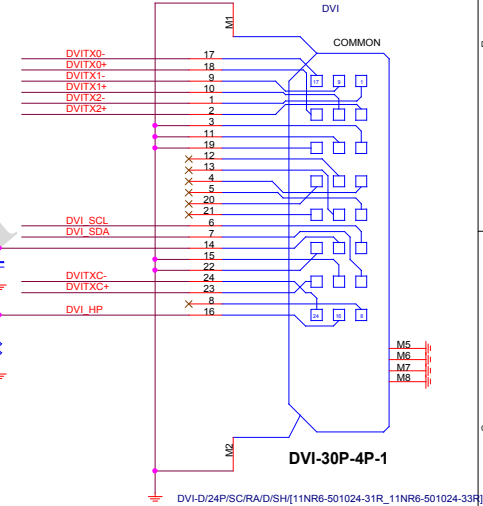
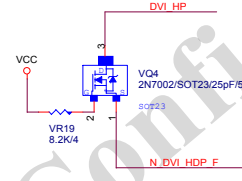
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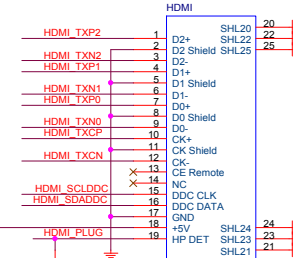
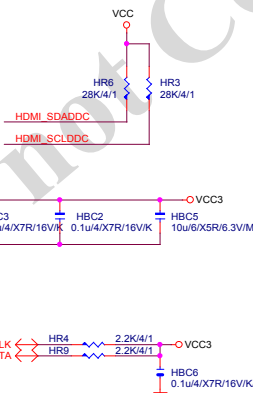
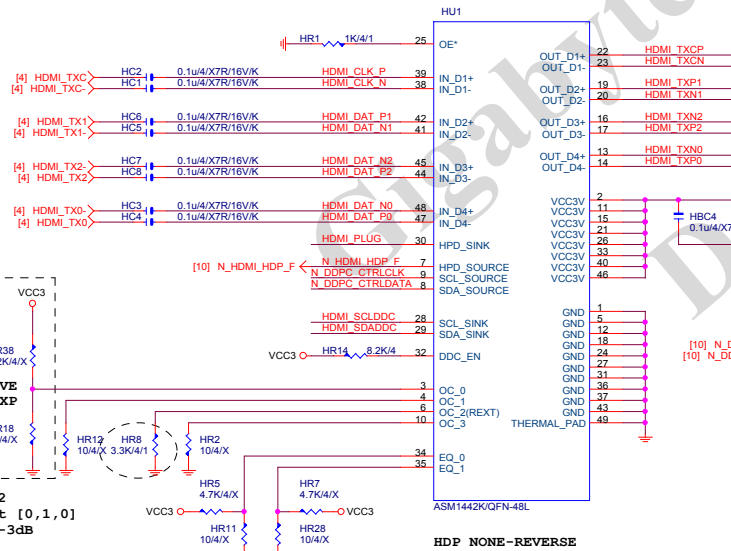


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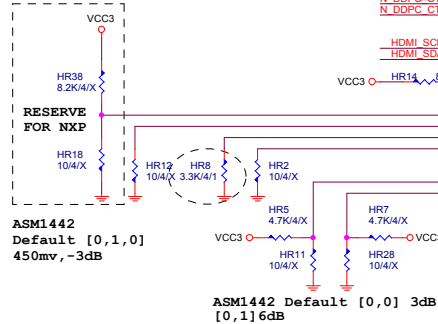


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HDMI LEVEL SHIFT



HDMI-3



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